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30-GHz MONOLITHIC RECEIVE MODULE TECHNOLOGY ASSESSMENT

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30 GHz Monolithic Receive Module
Final Technology Assessment Report

Contract No. NAS3-23356

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1.0 INTRODUCTION

This report is a technology assessment relevant to the 30 GHz Monolithic Receive Module development. It is based on results obtained on the present NASA Contract (NAS3-23356) as well as on information gathered from literature and other industry sources. To date the on-going Honeywell program has concentrated on demonstrating the so-called interconnected receive module which consists of four monolithic chips - the low noise front-end amplifier (LNA), the five bit phase shifter (PS), the gain control amplifier (GC), and the RF to IF downconverter (RF/IF) - as shown in Figure 1. Results on all four individual chips have been obtained and interconnection of the first three functions has been accomplished. Future work on this contract is aimed at a higher level of integration, namely, integration of the first three functions (LNA + PS + GC) on a single GaAs chip. The report presents the status of this technology andprojections of its future directions.

2.0 CURRENT TECHNOLOGY STATUS OF KA-BAND MONOLIHTIC CIRCUITS

In this section we describe the status of GaAs monolithic circuit technology, specifically in relation to the types of integrated circuits required for the NASA 30 GHz receiver. In at least two cases Honeywell has achieved first-time demonstrations of specific multi-transistor monolithic circuits at Ka-band. Such circuits are essential for 30 GHz receiver feed array applications such as those considered under the present contract as well as for future mm-wave phased array systems.

2.1 Low Noise FETs and Amplifiers

The current state of technology in low noise GaAs MESFETs is best assessed by scatter diagrams of gain and noise figure as shown in Figure 2. This figure shows GaAs MESFET gain and noise figure results reported in various papers. Since gain and noise figure measurements are reported over a range of frequencies, some basis for comparing the results is required. A 6 dB per octave gain roll off with frequency is commonly used for comparing FET gain. Noise figure results at various frequencies are compared using Fukui's noise equation [1] to generate a noise figure vs frequency curve for a hypothetical

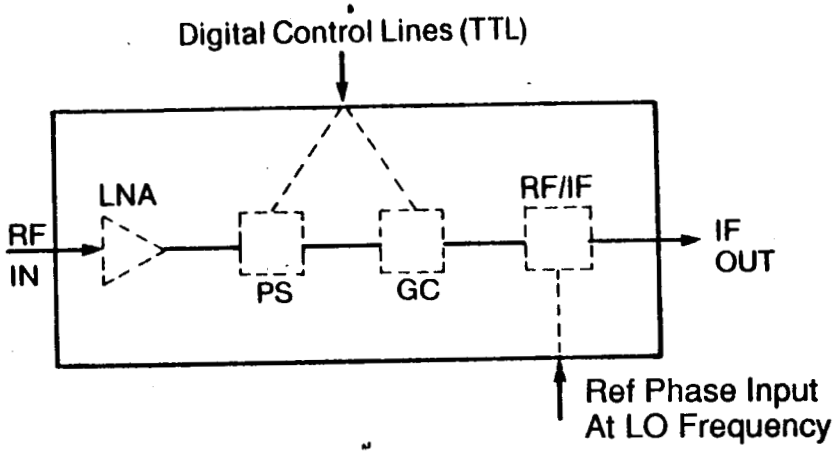

Figure 1. Submodule Functions of Interconnected Receive Module.

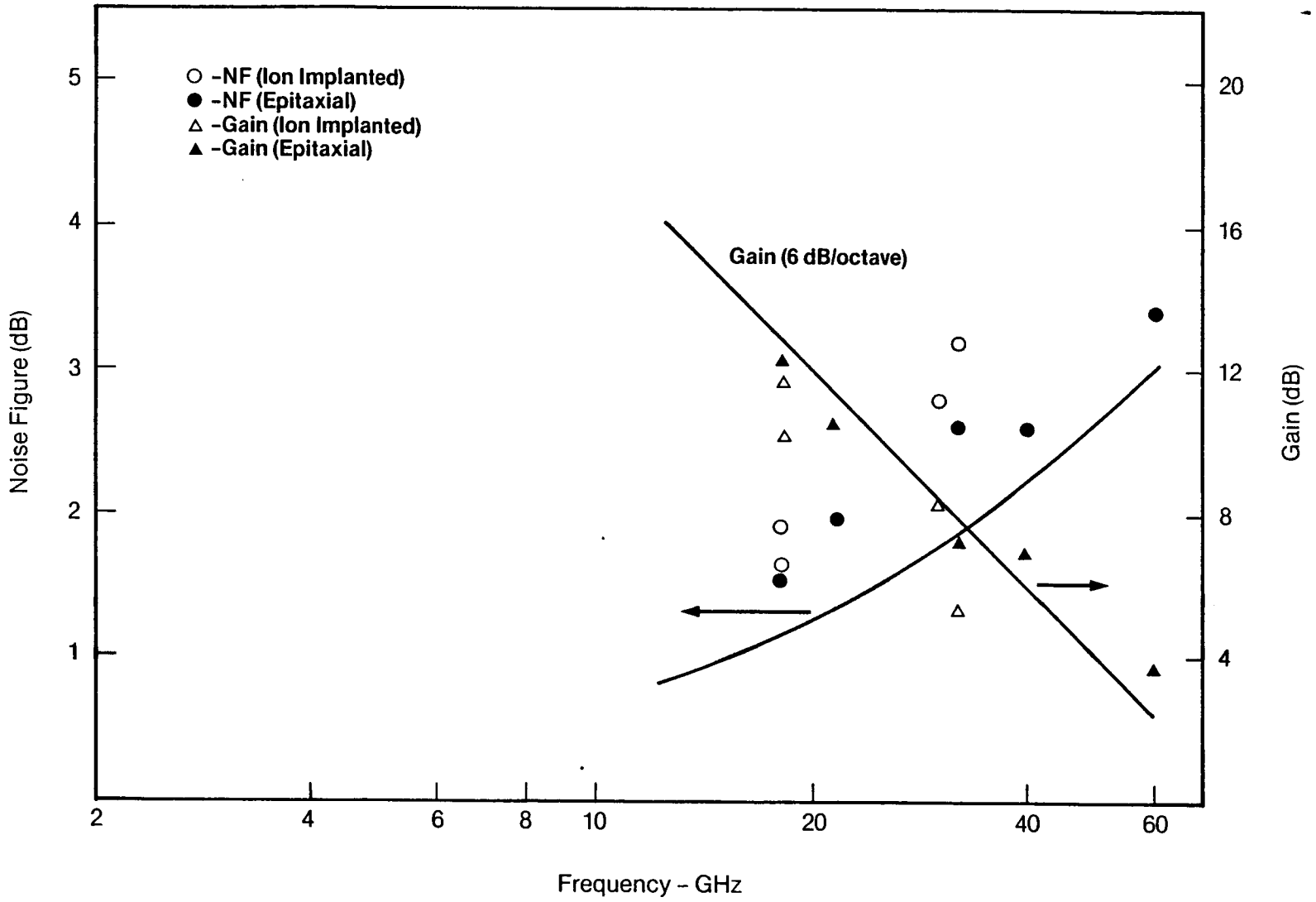

Figure 2. Gain and Noise Figure for GaAs MESFETs

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MESFET. Some care must be used in extrapolating noise figure results since some FET designs may not be suitable for higher frequencies [2]. As can be seen in Figure 2, typical gain and noise figure results for MESFETs indicate that spot noise figures of 3 dB with 8 dB of associated gain can be achieved at 30 GHz.

Results are shown for devices fabricated on both ion implanted and epitaxial material and these results indicate that state-of-the-art performance can be achieved using ion implanted devices. However, two notes of caution are in order:

- o The best ion implanted results were achieved by ion implantation into buffer layers.

- o Typical f_t's for ion implanted low noise FETs lag behind the f_t's of devices fabricated on epi material.

So, although ion implanted devices may offer adequate performance at Ka-band, they are not the best choice for high performance. Substrate material as well as intrinsic limitations of the ion implantation approach play a role in the reduced performance.

To date there have been few reports of monolithic low noise amplifiers at 30 GHz. Honeywell has achieved 7 dB noise figure with 6 dB gain at 30 GHz [3] and Hughes has achieved 7 dB noise figure with 14 dB gain [4,5] at Ka-band. Both results are considerably higher than the spot noise figures shown in Figure 2. There are a number of possible causes for the higher noise including the following:

- o Monolithic IC results are for circuits fabricated using direct ion implantation into LEC substrate material rather than ion implantation into a VPE buffer layer or epi material.

- o Spot noise figures quoted in the literature are corrected for fixture losses. Some of these losses are an integral part of a monolithic IC.

- o On-chip LNA matching networks may not be providing the optimum noise match and the on-chip matching networks are not easily modified.

- o Matching for the required bandwidth (27.5-30 GHz) may be different than the optimum noise match for the best spot noise figure.

We believe that all these considerations play a role in the poorer noise figures reported for monolithic ICs. Material considerations are probably a significant cause of the higher noise figure. This observation is borne out by our gain and noise figure measurements of discrete devices fabricated on the same wafer as the monolithic ICs. The best spot noise figure and gain results achieved to date are 4.6 dB and 3.8 dB respectively at 30 GHz. At 15 GHz, a gain of 7.2 dB with 1.9 dB noise figure was measured on devices from the same wafer. Honeywell presently has ongoing research investigating the effects of impurities and annealing techniques on the performance of Ka-band MESFETs. There is also a continuing effort investigating the matching requirements for best LNA performance. We believe this work will eventually lead to improved ion implanted monolithic ICs.

2.2 Gain Control and Phase Shifter Circuits

Gain control and phase shift circuits are necessary to achieve proper phase and amplitude distribution across the active elements of a phased array. For the 30 GHz receiver a 5-bit phase shifter and a gain control amplifier with five gain levels and an off state are required. Both functions are accomplished at the RF frequency because of system performance considerations [6].

Under the present 30 GHz receiver program, Honeywell has designed, fabricated, and evaluated monolithic 5-bit phase shifters and continuously variable two-stage gain control amplifiers (G_{max} ~ 12 dB) in the 27.5 - 30 GHz frequency range. To our knowledge these are the first such monolithic circuits to be reported in Ka-band. Tables 1 and 2 show a summary of the performance achieved on the monolithic phase shifter and gain control ICs respectively. A comparison is also made of the achieved performance versus the original program goals for the IC. As seen from the Tables, the basic circuit

TABLE 1

PHASE SHIFTER PERFORMANCE

Basic Performance Goals	Performance Achieved
Number of Bits: 5	5 (3 switched delay lines; 1 loaded line with continuous phase adjustment 0^{o} - 35^{o})
Accuracy: $\pm$ 3^{o} @ Band Center	$\pm$ 15^{o} (worst case)
Insertion Loss: 6 dB	8 dB
Maximum Gain Variation with Change in Phase State: 0.25 dB	$\pm$ 2 dB center band (worst case)
To Operate on TTL Input	Requires external controller
	Chip Size: 2.5 x 5.5 x 0.15 mm^3
	Number and type of transistors:
	Fourteen, 400 x 1 micron switching FETs (no drain bias applied)

TABLE 2

GAIN CONTROL AMPLIFIER PERFORMANCE

Basic Performance Goals	Performance Achieved
Gain (Max, Min): +12, -1 (dB)	+ 12 dB, at least -20 dB
NF: (Min, Max): 10, 14 (dB)	TBD
Gain Variation: Six Levels and Off State	Continuously variable and off state
Frequency: 27.5 - 30 GHz (1 dB BW)	29.5 - 30.6 GHz (2 dB BW)-unmodified [expect to achieve 27.5 - 30 GHz with modifications]
Maximum Phase Variation with Change in Gain State: Less than $\pm 5^{o}$	$\pm 10^{o}$ worst case across 27.5 - 30 GHz band for single stage. Measurements on two stage amplifier in progress
To Operate on TTL Input	Requires external controller
	Chip Size: 1.8 x 0.5 x 0.15 mm^3
	Number and type of transistors: Two, 100 x 0.25 micron dual gate FETs

performance has been achieved, although significant improvement in specific electrical tolerances is still required to meet the original performance goals.

Monolithic phase shifters and variable gain control amplifiers have also been reported at 20 GHz. A four-stage 0.5W dual gate amplifier has been developed for NASA as a variable power amplifier for the transmit branch of the satellite 30/20 GHz transceiver [7]. Similarly, a 5-bit switched line phase shifter has been developed at 20 GHz, which in addition incorporates a buffer amplifier to compensate for phase shifter loss [7]. Even more examples of similar type monolithic circuits exist at lower microwave frequencies; however, device and circuit requirements are considerably relaxed from comparable circuits at Ka-band. At the very least, 0.25 micron gate length FETs are a necessity at Ka-band to achieve reasonable gain performance. Honeywell's 0.25 x 100 micron dual gate FETs used in the monolithic gain control amplifier represent a state-of-the-art performance level achieved with such devices.

2.3 Mixer and IF Amplifiers

Mixers - The difficulty in describing the status of these devices is the variety of mixers which have been fabricated. These include:

- o Mixers integrated with other functions.
- o Wide vs narrow instantaneous bandwidth designs.
- o Operating frequencies from a few MegaHertz to 100 GHz.
- o Unbalanced, single balanced and double-balanced designs.
- o Diode or FET mixing elements.
- o Variety of transmission media.

The data describing these devices will be presented in tables. Table 3 contains the raw data, while Table 4 shows comparisons between the different mixer types.

Most of the diode structures are formed on material grown by vapor phase epitaxy (VPE) or molecular beam epitaxy (MBE) which makes further

TABLE 3

MONOLITHIC MIXER PARAMETERS

Mixer	Conversion Loss (dB)	Signal Frequency (GHz)	Intermediate Frequency (GHz)	Type	Transmission Medium	Size (mm x mm)
1	6 to 8**	0.1 - 0.8	0.1	FET Implanted	Lumped Element	0.75x0.75
2	8.0	10.7	1.0	Diode Implanted	Microstrip	2 x 2.25*
3	6.0	14-20	2-8	FET Implanted	Microstrip	2.2 x 2.6
4	6.0	30	1.0	Diode MBE	Coplanar	NA
5	6.0	31	1.5-2.8	Diode VPE	Microstrip	2.5 x 5*
6	6.0	31	0.1	Diode VPE	Waveguide	1.3 x 10
7	6.5	34-36	0.25	Diode VPE	Microstrip	NA
8	0.0	44.5	3.0	HEMT	Hybrid Microstrip	Not Monolithic
9	6.5	60	1-4.5	Diode Implanted	Microstrip	NA
10	7.5 9.0	76 84.6-93.1	15.5 0.5-8.5	Diode VPE	Waveguide	NA
11	4.6 ~ 8.0	91.1 73.6-83.6	< 1.0 8 - 18	Diode VPE	Slotline Coplanar WG	2 x 2
12	7.1 < 10.5	94.5 93 - 96	0.1 0.1	Diode VPE	Microstrip	2 x 0.9
13	3.8	110	1.2	Diode VPE	Quasi-Optic VPE	1.3 x 2.5

* Includes IF Amp

** This number is conversion gain due to use of FET in mixer.

TABLE 4

COMPARISON OF MONOLITHIC MIXERS

Mixer	Configuration	Advantages	Disadvantages
1	Double balanced discrete FET mixer IC	Good intermodulation characteristics	Low frequency device for UHF
2	Lumped element balanced diode mixer	Small size FET compatible	Bandwidth
3	Distributed FET image rejection	Bandwidth FET design	Power consumption
4	Balanced/unbalanced transmission line diode mixer on MBE	Potential bandwidth and electrical performance	Not readily compatible with FETs, large area and expensive processing material
5	Quadrature hybrid VPE diode mixer with VPE FET IF	Integrates FET and diodes on same substrate	Complex fabrication process, low yield, narrow bandwidth
6	Monolithic crossbar mixer in metal waveguide	Potentially wide bandwidth	Fragile, expensive, low process yield, mounting critical
7	Quadrature hybrid VPE diode mixer	Dual circuit function	Low process yield, narrow bandwidth
8	Single-ended HEMT hybrid construction (not monolithic, but could be)	Potential integration with HEMT amplifier	Complex material growth and limited bandwidth
9	Quadrature hybrid diode mixer formed by ion implantation	Simple integration of FETs and diodes	Limited electrical performance compared to VPE material

TABLE 4

COMPARISON OF MONOLITHIC MIXERS

Mixer	Configuration	Advantages	Disadvantages
10	Monolithic crossbar VPE diode mixer in metal waveguide	Wide bandwidth operation	Fragile, expensive, relatively low process yield, mounting critical
11	Slotline/coplanar stripline diode balanced mixer	Broad bandwidth and small size	Mounting critical with somewhat difficult interfaces
12	Rat race hybrid VPE diode mixer	Moderate bandwidth and small size	Not easily integrated with FETs, difficult process
13	Quasi-optic single-balanced diode mixer	Simple interface and good performance	Large size, fragile, requires very quiet local oscillator

integration very difficult [11]. This is one of the benefits of using selective ion implantation to make mixer diodes. In this case, very few additional processing steps are needed to make field effect transistors which are useful for amplifiers and many other devices [9,12,16]. Of course, the device which is most compatible with fabrication of FET based circuits is the FET mixer itself.

Generally FET monolithic mixers have been designed for use at lower frequencies where their high IF output impedance is not as significant a matching problem as it is at higher frequencies [8]. There are also applications where the FET output impedance can be reduced by paralleling multiple devices for a wider bandwidth and higher IF frequencies [10]. While not yet implemented in monolithic form, configurations using HEMT devices also appear to be promising for integrating amplifiers with mixers in the future [15].

IF Amplifiers - While many monolithic amplifiers of various kinds have been fabricated, not many have been integrated with mixers. The characteristics of the few that have are indicated in Table 5. All of these designs employ a single stage and, with the possible exception of Reference 9, are intended to demonstrate feasibility rather than provide significant functionality.

3.0 OPTIMUM MODULE FABRICATION PROCESSES AND TECHNOLOGIES

This section begins with a description of the Honeywell fabrication process which will be used to develop NASA's Cascaded Two-Submodule (CTS) 30 GHz receiver. For the CTS receiver our approach is to integrate on the same chip three RF circuits consisting of the LNA, phase shifter and gain control amplifier. The second submodule chip integrates a diode mixer and an IF amplifier. Since each of these monolithic circuits nominally requires different types of FET devices, a highly flexible fabrication process capable of selective doping is required. Additionally, the process must ultimately achieve high performance, yield and repeatability if such monolithic 30 GHz circuits are to become practical for actual system implementation. We believe the present Honeywell approach which is based on ion implantation and hybrid (optical projection/e-beam) lithography on 3-inch substrates, is today best

TABLE 5

MONOLITHIC MIXER/IF AMPLIFIERS

Reference	Gain (dB)	Noise Figure (dB)	Bandwidth (GHz)	Power (mW)
2	> 10	< 3	0.5 - 1.3	120
5	10	< 3	2.0 - 3.0	NA
9	3	3	1.0 - 4.5	NA

able to fulfill the above requirements.

New technology; however, is emerging which holds promise for improved performance, especially in terms of low noise amplification. HEMT (high electron mobility transistor) technology, which requires special epitaxial growth techniques, has the potential for achieving receiver noise figures of 3 to 4 dB at 30 GHz. However, HEMT monolithic technology is now in its infancy and it is unclear whether monolithic integration of several circuit functions can be achieved cost effectively. Nevertheless, HEMT amplifier chips can be used separately, for example, as the front-end LNA to establish (set) the receiver noise figure. We discuss this possibility in the latter half of this section.

3.1 Honeywell's Censor/E beam (Submicron FET) Fabrication Process

A flowchart of the key steps in Honeywell's Censor/E-beam fabrication process is shown in Figure 3. This is an extremely flexible process for fabricating submicron devices and ICs for high-frequency (1.0 - 100 GHz) and high-speed logic applications. It is based upon advanced "hybrid" lithography, combining 10:1 projection optical lithography with electron-beam lithography.

Because of the process's flexibility, it can fabricate Schottky-barrier mixer diodes as well as MODFETs and MESFETs for MIMIC applications. Honeywell's processing approach produces more chips per 3-inch wafer than a 2-inch wafer processing approach. Also, using optical projection lithography instead of contact lithography ensures a higher yield of functional chips per wafer. Consequently, Honeywell's process will ultimately result in reduced cost per chip.

Frontside Processing - Starting substrates for Honeywell's Censor/E-beam process are 3-inch, undoped, semi-insulating, LEC GaAs wafers. Because of its flexibility, the process can form the device active layer on such substrates by either SELECTIVE ion implantation, BLANKET ion implantation, or epitaxial growth (MBE, VPE, MOCVD).

Using electron beam lithography to fabricate the FET gates allows excellent

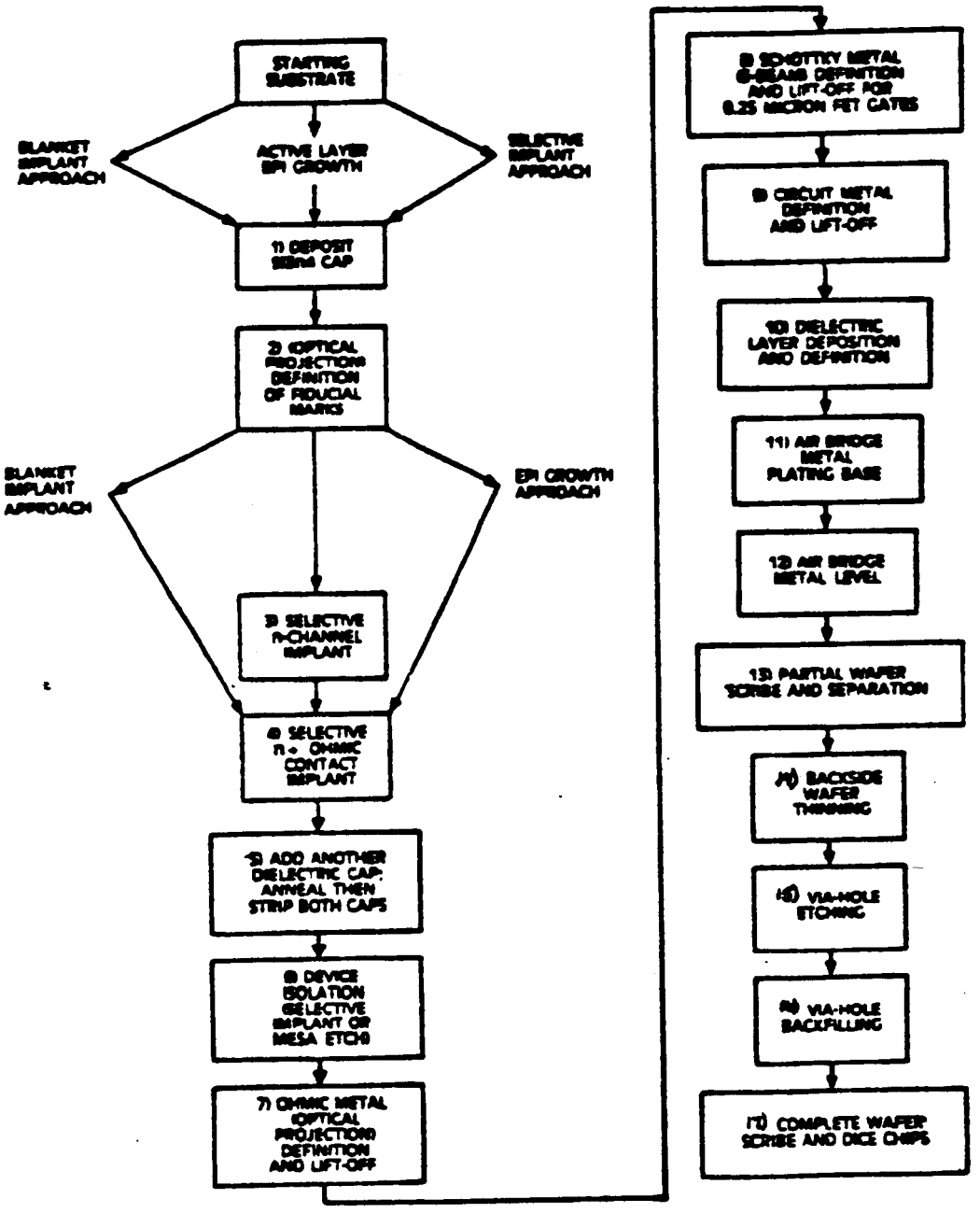


Figure 3. Flowchart of the key steps in Honeywell's submicron-FET MIMIC fabrication process.

control of the critical FET gate lengths down to ~0.25 micron. The device gate metal structure is fabricated using lift-off and PMMA electron-beam resist to achieve 0.25 micron linewidths. The e-beam system (Cambridge EMBF-6) is used ONLY for fabrication of the submicron (0.25 micron) MESFET gate, minimizing any processing bottleneck due to electron-beam lithography.

The other frontside mask levels are defined entirely by using a Censor SRA-100, direct step on wafer (DSW), 10:1 projection, alignment/exposure system. This state-of-the-art optical lithography system is instrumental in obtaining the chip yields necessary for a feasible submicron-FET process. The Censor system has been intermixed successfully with the Cambridge e-beam system to establish the lithographic component of the process.

Mesa etch or selective ion implantation (proton or oxygen ions) provide isolation between devices on the processed wafers. Ohmic metalization for the source and drain contacts is performed using a two layer resist (photoresist and PMMA) liftoff process. The electron beam deposited ohmic metal is a Au-Ge (eutectic)/Ni layer which is alloyed after liftoff. The critical FET gate metal structure is fabricated using PMMA electron-beam resist to achieve 0.25 micron linewidths. After electron-beam exposure and development, the gate recess is wet-chemically etched. The gate metal is then electron-beam deposited and lifted off. Figure 4 displays data for 0.25-micron MESFETs on 3-inch wafers processed using Honeywell's submicron-FET fabrication process.

The circuit metal layer is defined by projection optical lithography and two-layer resist on the Censor system. The circuit metal is then electron-beam deposited and patterned by liftoff. This metal also forms the bottom plate for the on-chip capacitors. Plasma CVD silicon nitride is deposited for on-chip capacitors and FET passivation dielectric. The deposited nitride is defined afterwards by dry etching in a planar plasma etcher, typically producing capacitances of 15,000 pF/cm^2.

The air bridge metal plating base forms part of the on-chip capacitor top plate as well as the plating base for the air bridge crossovers. The air bridge metal plating base is sputter-deposited onto a photoresist pattern. The air bridge structures are formed by applying and patterning a second layer

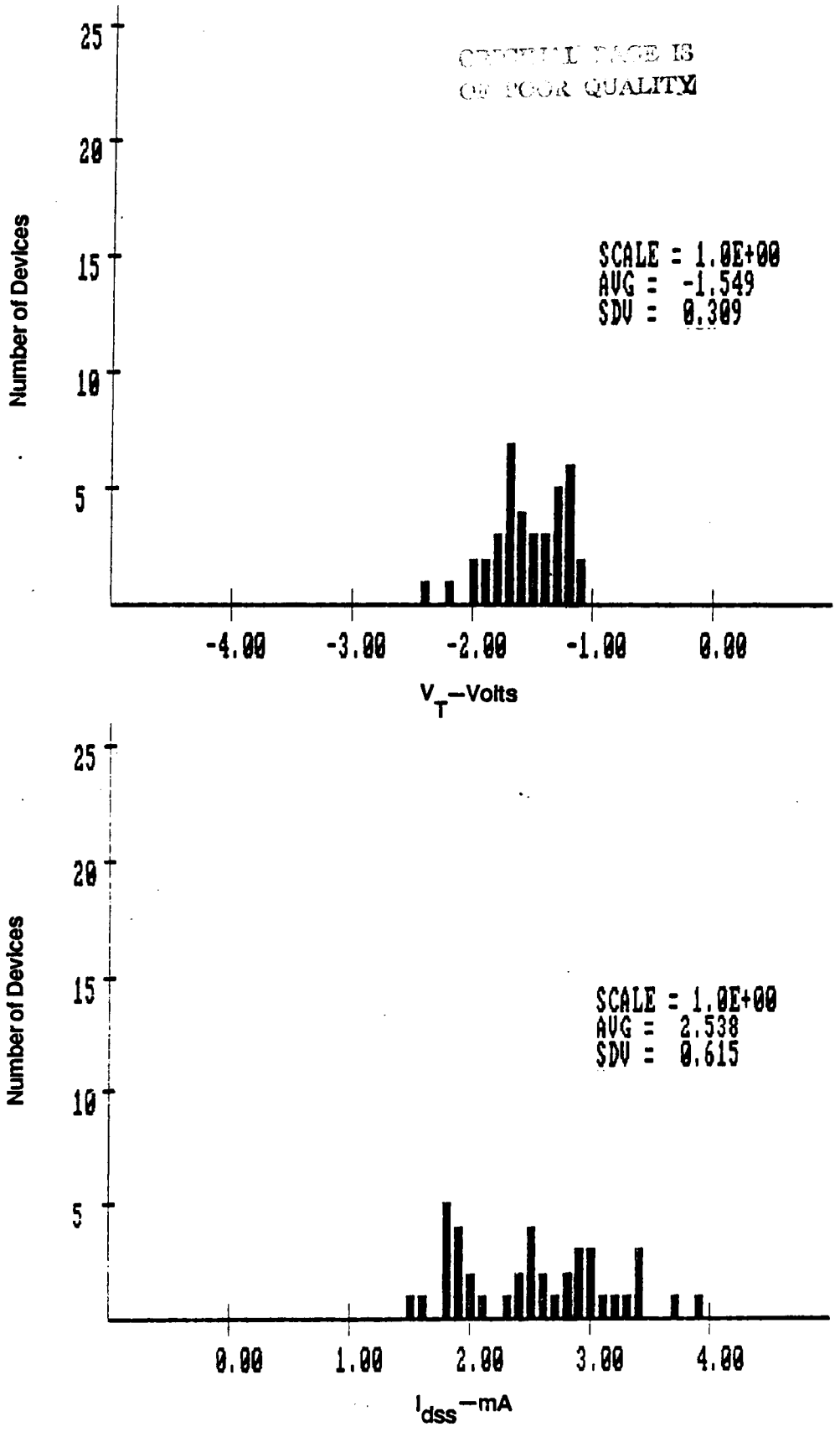


Figure 4. Data for 0.25-micron MESFETs on 3-inch, MIMIC wafers produced using Honeywell's submicron-FET, MIMIC fabrication process.

of resist on top of the plating base metal layer.

Afterward, a thick gold layer is electroplated, comprising the device and circuit air bridges, the top plates of the on-chip capacitors, and the circuit interconnects. After plating, the resist layers are removed by solvent stripping and the plating base metal is removed by ion milling.

Backside Processing and Substrate Via Hole Definition - The backside processing in Honeywell's process consists of thinning the GaAs wafers to 4-6 mils thickness, etching via holes through the substrates, and backfilling the substrate via holes with metal. This processing is crucial since the chip yield, particularly for large ICs, can be significantly reduced by wafer breakage or damage during these steps.

The use of via-holes through GaAs substrates is important for improving the high-frequency performance of microwave and millimeter-wave devices and ICs. Honeywell has developed the capability to etch via holes in thinned (4-6 mil thick) GaAs substrates by ion-beam-assisted etching (IBAE) [21].

The IBAE technique (Figure 5) utilizes the interaction between an argon ion beam impinging upon a GaAs substrate and a stream of reactive gas independently directed onto the substrate to achieve rapid and highly-anisotropic etching of the GaAs substrate. Typical 50 micron x 75 micron etched via holes possess vertical sidewalls with no mask-undercutting. After etching, they are backside-filled by metal sputter-deposition and electroplating.

Recently, we have achieved high DC yields for continuous backside-to-frontside via contacts in processed test wafers. On four different via hole test wafers, we achieved yields of 100%, 96%, 88%, and 94%, respectively. The test wafers also had low enough frontside-to-backside impedances to indicate that good RF behavior can be obtained.

Wafer Dicing - The final backside processing step involves dicing the wafer into individual chips for mounting, testing, and delivery. Honeywell uses a scribe and break technique for dicing with minimum edge damage to the chips.

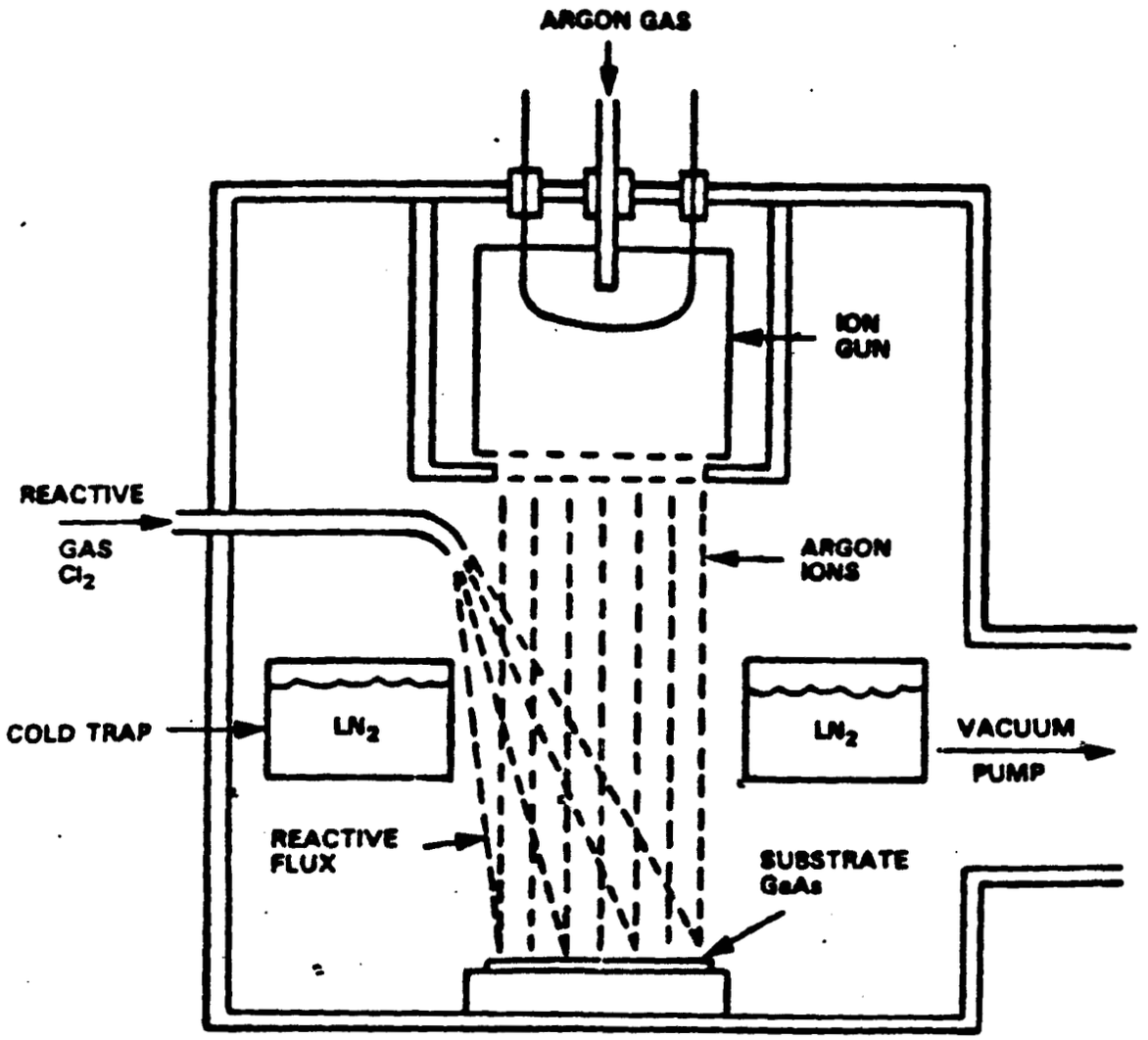


Figure 5. Schematic diagram of Ion-Beam-Assisted Etching (IBAE) technique for high-resolution etching of MIMIC substrate via holes.

The wafer scribing is done on a Loomis MKT-38 scriber. Afterwards, it is mounted on a plastic sheet, roller-broken along the scribe lines, and stretched on a SEC Model 2600 die matrix expander to separate the dice for selection and packaging. This is a rapid, high-yield approach to wafer dicing.

3.2 Ion Implantation vs HEMT for High Performance

One alternative to a single receiver IC is segmentation of the receiver into several ICs according to the device types required for the various subcircuits. Tradeoffs between cost and performance are the basis for partitioning the receiver into subcircuits. A specific example of such a tradeoff involves the low noise amplifier section of the receiver. Recent results [22,23] show that the modulation doped FET or MODFET (also known as the HEMT, TEGFET or SDHT) with a GaAs channel layer offers a significant improvement in noise figure and gain over the conventional FET. The most recent results using an InGaAs channel material show still further improvement over the conventional GaAs/AlGaAs MODFET. Typical state-of-the-art gain and noise figure results are shown in Figure 6 for both the conventional MESFET and the GaAs/AlGaAs MODFET. Based on these results, a MODFET low noise amplifier would offer a noise figure improvement of at least 0.5 dB at 30 GHz compared to the conventional FET. Some improvement in gain and ease of matching might also be realized with MODFETs. However, the channel layer for the MODFET is normally grown by molecular beam epitaxy (MBE) which is more expensive than direct ion implantation into semi-insulating substrate material. Also, the MBE channel layer is less versatile than the ion implanted approach in terms of integrating a variety of device types on a single IC. Typically the MODFETs are low current devices which is an advantage from the standpoint of power dissipation but the MODFET channel layer would not make a good switching device for phase shifting due to its high ON resistance. Thus, future developments might result in high performance receivers with a low noise amplifier, and perhaps gain control amplifier subcircuits separated from the phase shifting and RF/IF functions. The amplifier and gain control subcircuits would be fabricated on MBE material; the phase shifter and RF/IF function on ion implanted material. On the other hand, if extremely low cost with high volume production is a

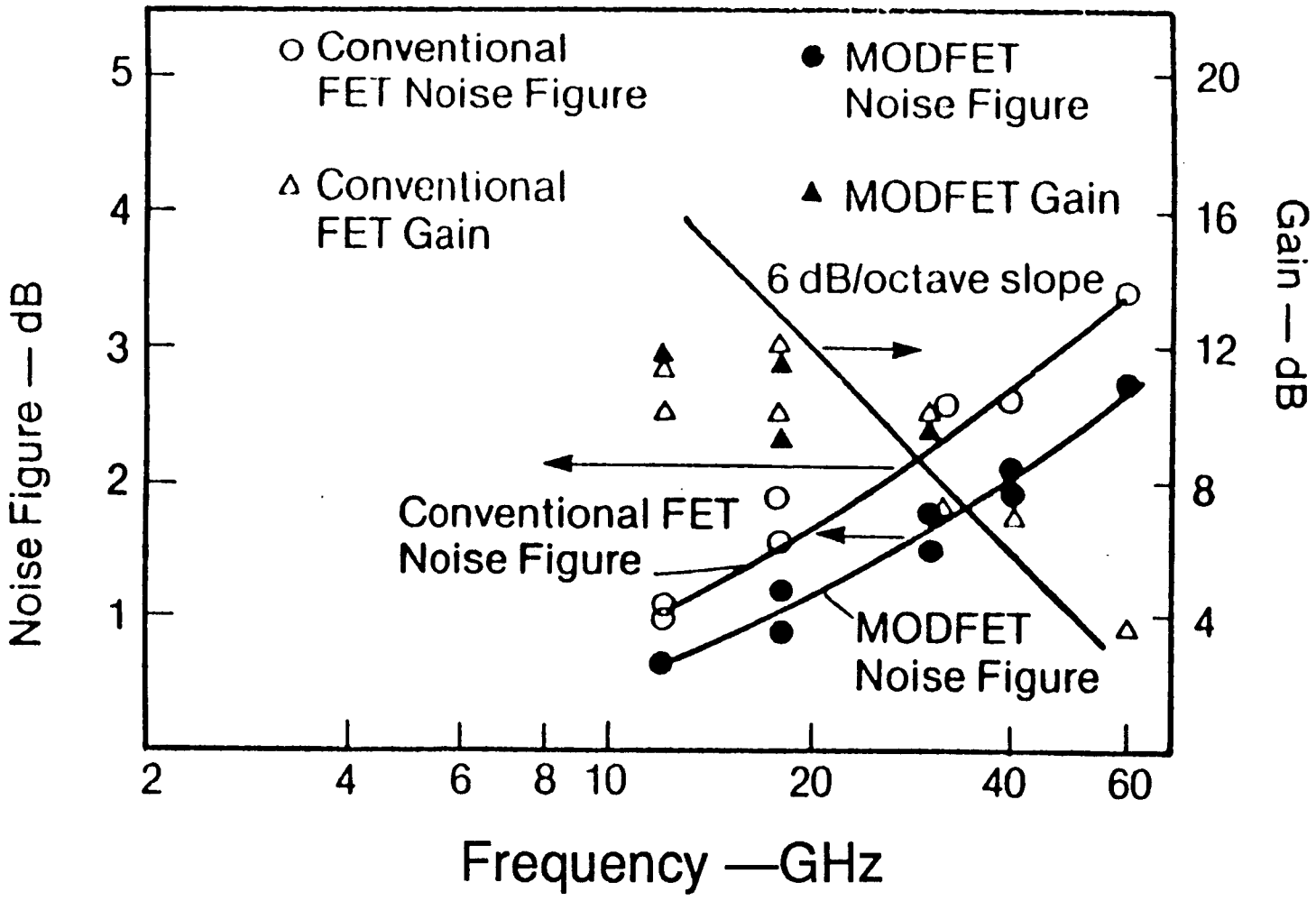


Figure 6. Noise Figure and Gain Comparison of Conventional FETs and MODFETs.

dominant factor, the whole receiver might be fabricated on ion implanted material. Future developments in this area will depend on demonstration of MODFET devices with reproducible performance from wafer-to-wafer and low light sensitivity. The development of material growth technology will strongly influence the cost and potential for high volume production.

4.0 TECHNOLOGY GROWTH POTENTIAL

4.1 Materials

The general material approach for fabricating 30 GHz receiver circuits is to define a GaAs active lasyer on a semi-insulating GaAs substrate. Two general areas of materials approaches can be identified for forming the active layer:

- o Selective ion implantation of dopant ions directly into the semi-insulating substrate.

- o Growth of the active layer onto the semi-insulating substrate by epitaxial techniques such as MBE (Molecular-Beam Epitaxy), VPE (Vapor Phase Epitaxy), LPE (Liquid-Phase Epitaxy), or by the less-mature epitaxial technique of Metal-Organic Chemical Vapor Deposition (MOCVD).

Selective ion implantation is often used as the materials technique utilized for GaAs IC fabrication. It offers the following advantages:

- o Low-cost compared to most epitaxial materials approaches.

- o High-throughput achieved through the performance of commercial implanters.

- o High throughput achieved because of the uniformity and reproducibility of commercial implanters and annealing systems.

- o Monolithic integration capability, including the flexibility to fabricate devices with different properties on the same IC.

For 30 GHz applications, however, the usefulness of selective ion implantation is constrained by the following device and materials considerations:

- o 0.25-micron-gate MESFETs need thin, heavily-doped active layers to produce short effective device gate lengths.

- o An abrupt doping transition (> 400A/decade) must be achieved at the active layer/substrate interface.

- o The device's properties should be determined entirely by the properties of the active layer and not by any peculiarities of the semi insulating substrate.

- o Heavy doping (> 3.0 E17/cm^3) of the device active layer is desired with accompanying good electron mobility.

Although the use of selective ion implantation is constrained by these considerations, the following additional factors suggest it will still find application as a 30 GHz materials apoproach:

- o Processing techniques are being developed to improve the characteristics (e.g., doping levels, doping profiles, substrate/active-layer transition) of ion-implanted material compared to epitaxial material.

- o Device requirements at 30 GHz may allow the use of lower-performance implanted materials in place of epitaxial materials.

- o Material vendors are consistently improving the quality of their semi-insulating substrates; combined with improved substrate qualification techniques, this should minimize the effect of substrate quality on device properties.

- o There exists strong potential (via innovative processing techniques such as rapid thermal annealing) for combining implantation with epitaxial growth as a 30 GHz materials apoproach.

The device and materials requirements listed above are satisfied, in general, by the epitaxial materials approaches to defining the active layer. LPE, however, produces inferior surface morphology and can only produce uniform growth over a limited substrate area [24]. VPE achieves good surface quality and uniformity but cannot be readily extended to produce heterostructures, an important research and development area for exploiting the potential of GaAs [24].

MOCVD overcomes these problems and promises high-throughput, low-cost growth of epitaxial layers. Unfortunately, it also has exhibited difficulty in producing good semi-insulating buffer layers with background doping near 10 E14/cm^3. MBE overcomes most of these problems and allows more abrupt doping transitions than with MOCVD. Throughput, however, has been a major drawback with MBE due to the slower growth mechanisms employed.

It should be clear from these considerations that trade-offs must be made in determining the materials growth approaches for 30 GHz applications. No single technique has emerged as dominant and generic enough for all application areas. For example, selective ion implantation will retain an important role despite its performance disadvantages compared to the epitaxial approaches. Also, among the epitaxial approaches, competition between the favored MBE and MOCVD approaches is heating up as technological advances continue to improve both the throughput for MBE systems and the quality of MOCVD material.

4.2 Devices

Ion implantation is the approach for fabricating the active devices in this program. This is still a good, conservative, approach but the performance of the receiver can be enhanced by employing more advanced material growth techniques. Some potential device candidates for amplifiers and mixers are:

- o GaAs AlGaAs high electron mobility transistors (HEMTs) [25].
- o Pseudomorphic InGaAs/AlGaAs modulation-doped field effect transistors [26].

- o Advanced design field effect transistors fabricated using molecular beam epitaxy [27].

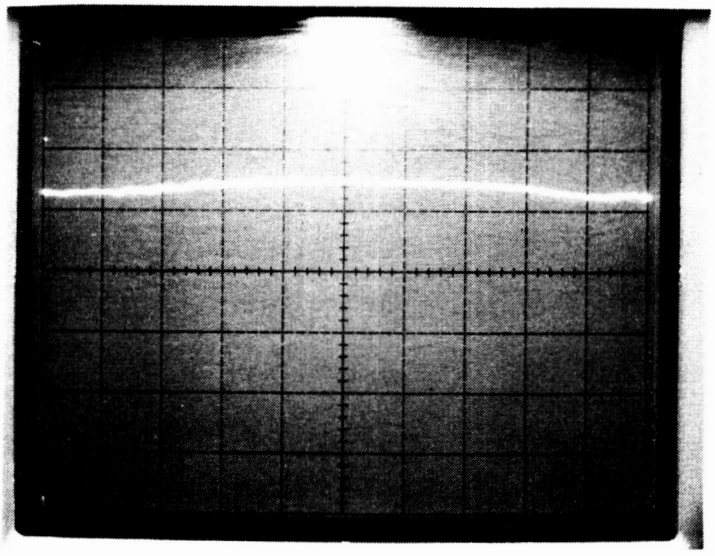
The performance of these devices as measured in our own and other laboratories is extremely promising for operation at millimeter wavelengths. As an example, some of the first simple recessed-gate discrete millimeter wave HEMTs fabricated on material grown at Honeywell have demonstrated the results shown in Figure 7. While these results are encouraging, there are presently some questions about the reliability of the first generation devices which have been fabricated at a number of laboratories. Modifications of the growth conditions or device structures will probably be necessary to solve these difficulties. A tool which may be useful in this regard is presently installed in our laboratories. It is a third generation MBE machine made by Physical Electronics (PHI 430) with a broad range of growth and diagnostic capabilities. This, and an earlier generation machine are available for fabrication.

Once the device structures are optimized, they will be incorporated in monolithic integrated circuit fabrication processes running in our laboratories.

4.3 Monolithic Circuits

The potential for technology growth in the circuits area is quite positive from at least three perspectives. First, MESFET based technology is continuing to develop in terms of increased integration capability. Second, new device technology such as the HEMT is extending device performance levels to higher frequencies and the potential for FET-based monolithic circuits at 100 GHz is not an unrealistic expectation. Third, substantial government sponsored programs such as the MIMIC project are promising to address the problem of fabrication of monolithic microwave integrated circuits on a large scale with emphasis on process repeatability and IC manufacturability.

For MESFET-based circuitry selective ion-implantation technology continues to offer the most flexibility in terms of monolithic integration of various

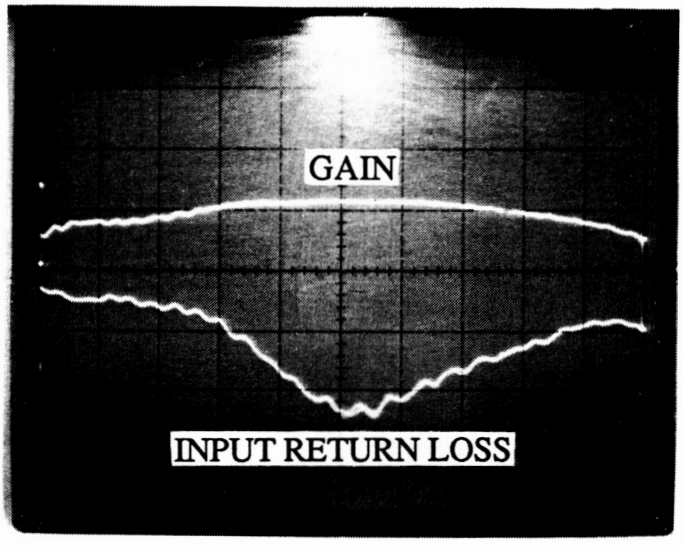


MODFET GCG9

VERT: 5dB/DIV

HOR: 27.5 - 32.5 GHz

REF: CENTER LINE



MODFET GC70

VERT: 5dB/DIV

HOR: 27 - 37 GHz

REF: CENTER LINE

N.F. = 5.1 dB

Figure 7. Early HEMT Amplifier Results with a Simple Gate Structure.

circuit functions requiring different device types. Not only RF functions need to be integrated, but digital circuits that interface various control signals with the RF circuitry also require monolithic integration. Such circuits together with more sophisticated on-chip bias distribution and filter networks will greatly reduce the number of ancillary bias and control wires necessary to operate the receiver chip(s). Performance and chip to chip circuit repeatability are also expected to improve with increased integration.

For Ka-band circuits monolithic integration to date has been restricted to demonstrations of specific RF functions (amplification, phase shifting, etc.). Emphasis has been placed on process development and achieving basic RF functionality. More sophisticated levels of integration will come about with process stabilization and repeatability of RF performance. In this regard programs emphasizing manufacturability and affordability (e.g., the DoD MIMIC program) will contribute greatly to the Ka band monolithic technology, provided efforts are equally focused at these frequencies as at lower microwave frequencies.

Other material technologies offer possibility for improved monolithic circuit performance. Especially significant will be circuits incorporating heterostructures such as the HEMT. Although requiring more restrictive epitaxial growth procedures, such as molecular beam epitaxy (MBE), these devices coupled with sub-half micron FET gates are expected to provide circuit functional complexity at 100 GHz comparable to what is today achievable at 10 GHz using monolithic MESFET technology. Development efforts will initially be focused on device characterization, modeling, and process development. Of particular importance will be reliability studies of such devices and development of process improvements which ensure device and circuit repeatability. For 30 GHz low noise receivers, HEMT-based monolithic chips may initially be used for special purpose applications.

5.0 30 GHz RECEIVE MODULE PERFORMANCE PROJECTIONS

An estimate of future module performance is made based on recent results achieved at Honeywell and other laboratories working on 30 GHz monolithic circuits, as well as on projections of new technology emerging in this area.

We assume the basic configuration of the CTS receiver as shown in Figure 1.

In the two to five year time frame basic functionality of the 30 GHz receiver will be achieved, especially for the case of the CTS receiver wherein the receiver function is implemented on two chips, an RF chip (LNA, PS, and GC) and a downconverter chip (mixer, IF buffer amp and LO buffer amp). An overall receiver noise figure of 5 tdo 7 dB can be expected using an all-ion-implanted approach. Improvements in ion-implanted materials preparation and circuit modeling, especially in terms of noise characterization, are assumed. In the five year time frame it can be expected that stabilization of fabrication processes and improved circuit designs that are more tolerant of process variations will improve receiver characteristics such as gain flatness vs. frequency, minimum phase variation with gain control (and vice versa), noise figure variation with frequency, etc.. We expect the receiver performance in the next five years to be somewhere between what has been achieved to date and the original, very ambitious, goals set forth in the NASA 1982 RFP. Special emphasis must be placed on integration of interface control circuitry and on-chip bias filtering and distribution networks that greatly reduce the number of auxiliary bias wires necessary to operate the receiver. Provided a continued effort is maintained that equals or exceeds the present receiver development, new heterostructure device technology is very likely to be introduced into the 30 GHz monolithic receiver in the next ten years. Parallel efforts including developing the new device technology as well as continued work in stabilizing fabrication processes must be accomplished if receiver performance and circuit repeatability are to be achieved. The important issue of efficient module control including on-chip digital control circuitry, bias distribution and filtering must be thoroughly addressed if receiver modules of this type are to become practical for actual system implementation. Using available current data on modulation-doped FETs it can be expected that monolithic receiver noise figures of 3-4 dB will be achieved. Again, the degree to which the original RFP goals are met are strongly dependent on the emphasis that is placed on achieving process and circuit repeatability.

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15. Supplementary Notes

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16. Abstract

This report is a technology assessment relevant to the 30 GHz Monolithic Receive Module development. It is based on results obtained on the present NASA Contract (NAS3-23356) as well as on information gathered from literature and other industry sources. To date the on-going Honeywell program has concentrated on demonstrating the so-called inter-connected receive module which consists of four monolithic chips - the low noise front-end amplifier (LNA), the five bit phase shifter (PS), the gain control amplifier (GC), and the RF to IF downconverter (RF/IF) as shown in Figure 1. Results on all four individual chips have been obtained and inter-connection of the first three functions has been accomplished. Future work on this contract is aimed at a higher level of integration, namely, integration of the first three functions (LNA + PS + GC) on a single GaAs chip. The report presents the status of this technology and projections of its future directions.

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